Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method for testing a DDR DRAM having a test mode and an operational mode, comprising in the order recited:

(a) placing said DDR DRAM in test mode;

(b) issuing a bank activate command to select and bring up a wordline selected for write of said DDR DRAM;

(c) writing with auto-precharge, a test pattern to cells of said DDR DRAM;

(d) repeating steps (b) and (c) until all wordlines for write have been selected;

(e) issuing a bank activate command to select and bring up a wordline selected for read of said DDR DRAM;

(f) reading with auto-precharge, the stored test pattern from cells of said DDR DRAM; and

(g) repeating steps (e) and (f) until all wordlines for read have been selected.

[c2] The method of claim 1, wherein each of steps (b), (c), (e) and (f) each take one clock cycle.

[c3] The method of claim 1, further including before step (a), the step of heating said DDR DRAM to a predetermined temperature.

[c4] The method of claim 1, wherein said DDR DRAM is operating at a clock frequency below about one MHz in said test mode.

[c5] The method of claim 1, wherein an amount of elapsed time between writing to and reading from a storage cell accessible by a particular wordline and bitline combination does not exceed a retention time specification of said storage cell.

[c6] The method of claim 1, wherein peripheral logic circuits of said DDR DRAM are adapted to execute a write burst enable and a column address command one clock cycle earlier in test mode than in operational mode, adapted to execute an auto-precharge enable one-half clock cycle earlier in test mode than in operational mode, and having a column address latency of one clock cycle in test mode and two or three clock cycles in operational mode.

[c7] The method of claim 1, wherein:
said DDR DRAM is adapted to initiate, in a timed auto-precharge mode of said test mode, a precharge immediately after a falling edge of a clock cycle; and
said DDR DRAM is adapted to, in a non-timed auto-precharge mode of said test mode, to start an auto-precharge asynchronously after the falling edge of a

clock cycle and after a timer allows enough time for a write-back to said DDR DRAM.

[c8] A DDR DRAM having a low frequency and a high frequency operating mode, comprising:
a multiplicity of storage cells arranged in an array, each storage cell accessible by a wordline and a bitline; and
wherein peripheral logic circuits of said DDR DRAM are adapted to execute a write burst enable and a column address command one clock cycle earlier in low frequency operating mode than in high frequency operating mode, adapted to execute an auto-precharge enable one-half clock cycle earlier in low frequency operating mode than in high frequency operating mode, and having a column address latency of one clock cycle in test mode and two or three clock cycles in operational mode.

[c9] The DDR DRAM of claim 8, wherein said DDR DRAM is operating at a clock frequency below about 33 MHz in low frequency mode and at a clock frequency above about 33 MHz in high frequency mode.

[c10] The DDR DRAM of claim 8, wherein writing to a particular storage cell takes two clock cycles in low frequency operational mode and five clock cycles in high frequency operational mode.

[c11] The DDR DRAM of claim 10, wherein said DDR DRAM, during writing to said particular storage cell in low frequency mode is responsive to a bank activate command during a first clock cycle and responsive to a write with auto-precharge command during a second clock cycle.

[c12] The DDR DRAM of claim 10, wherein said DDR DRAM, during reading from said particular storage cell in low frequency mode is responsive to a bank activate command during a first clock cycle, responsive to a write command during a second clock cycle and responsive to a precharge command during a fifth clock cycle.

[c13] The DDR DRAM of claim 8, wherein reading from a particular storage cell takes four clock cycles in both in low and high frequency operational modes.

[c14] The DRR DRAM of claim 8, wherein:
said DDR DRAM is adapted to initiate, in a timed auto-precharge mode of low frequency operational mode, a precharge immediately after a falling edge of a clock cycle; and
said DDR DRAM is adapted to, in a non-timed auto-precharge mode of said test mode, to start an auto-precharge asynchronously after the falling edge of a clock cycle and after a timer allows enough time for a write-back to said DDR DRAM.

[c15] A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit adapted to be coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method for testing a DDR DRAM having a test mode and an operational mode, said method comprising the computer implemented steps of, in the order recited:
placing said DDR DRAM in test mode;
(b) issuing a bank activate command to select and bring up a wordline selected for write of said DDR DRAM;
(c) writing with auto-precharge, a test pattern to cells of said DDR DRAM;
(d) repeating steps (b) and (c) until all wordlines for write have been selected;
(e) issuing a bank activate command to select and bring up a wordline selected for read of said DDR DRAM;
(f) reading with auto-precharge, the stored test pattern from cells of said DDR DRAM; and
(g) repeating steps (e) and (f) until all wordlines for read have been selected.

[c16] The system of claim 15, wherein each of steps (b), (c), (e) and (f) each take one clock cycle.

[c17] The method of claim 15, wherein an amount of elapsed

time between writing to and reading from a storage cell accessible by a particular wordline and bitline combination does not exceed a retention time specification of said storage cell.

[c18] The system of claim 15, further including before step (a), the method step of heating said DDR DRAM to a predetermined temperature.

[c19] The system of claim 15, wherein said DDR DRAM is operating at a clock frequency below about one MHz in test mode.

[c20] The system of claim 15, wherein an amount of elapsed time between writing to and reading from a storage cell accessible by a particular wordline and bitline combination does not exceed a retention time specification of said storage cell.